REMARKS

New claim 13 has been submitted for consideration. Claim 13 is original claim 4 written in independent form. As discussed below, this claim is believed to be patentable over the art of record.

Claim Objections

Claim 1 has been objected to on the grounds that it is not clear whether the switching means recited in lines 3 and 5 are the same. Claims 1, 2, 3, 7, and 8 have been amended in the manner indicated in the claim listing in order to overcome this objection. Claim 1 has also been amended to indicate that the first and second switching means are connected to the circuit node of interest "via a first pin of said IC" and "via a second pin of said IC", respectively.

Claim 9 has been amended to depend from claim 2 in order to provide proper antecedental support for the term "second stimulus voltage".

Claim Rejections - 35 USC 103

Claims 1-6 have been rejected under 35 USC 103(a) as being unpatentable over admitted art in Figs. 1-2 of Applicant's specification in view of Hashimoto U.S.P. 6,313,657. The Examiner is respectfully requested to reconsider the rejection in light of the following comments.

The Present Invention

The present invention seeks to provide a circuit and a method for accurately delivering DC or AC stimulus voltage to nodes "within an IC". The solution proposed by Applicant includes, within the IC, switching means for conveying a force voltage to a circuit node of interest "via a first pin of said IC" and for conveying a sense voltage from the circuit node of interest "via a second pin of said IC". These features are set forth in amended claim 1.

As indicated below, neither the admitted art nor the cited art discloses connecting the force and sense paths to a node of interest via two pins of the IC. Further, as admitted by the Examiner, the admitted art does not teach "means for selectively simultaneously enabling both of said switching means to enable said first stimulus voltage to be delivered to said one of said circuit nodes".

Admitted Art

The admitted art referenced by the Examiner is described in paragraph [0003] on page 1 of Applicant's specification. The switching means of the admitted art is external of the IC and is connected to one pin or terminal of the IC, not to internal nodes within the IC "via a first pin of the IC" and "via a second pin of the IC". The drawbacks of the admitted art are described at lines 30-35 of page 1 of Applicant's specification as follows:

> "While these arrangements succeed in accurately delivering a desired voltage to an IC pin, it does not deliver the desired voltage to the circuit node of interest within the circuit. More specifically, the arrangements do not accommodate voltage drops which may occur between the IC pin and the node of interest. It also does not provide a way of applying a high frequency voltage signal." (emphasis added).

Hashimoto

Hashimoto is concerned with an IC testing apparatus and with a very specific problem and objective, which are not related to those with which Applicant is concerned. The problem is discussed at col. 4, lines 10-12:

> "For these reasons, where semiconductor switches are used as the switches S1 and S2, there results a disadvantage that an overload test can not be conducted."

The objective of the Hashimoto invention is stated at col. 4, lines 13-18, as follows:

> "It is an object of the invention to provide an IC testing apparatus connected to an output of a DC tester and incorporating semiconductor switches as a first switch S1 and a second switch S2 which may connect

> the DC tester to a terminal of an IC under test or to interrupt such connection while enabling an overload test during a DC test." (emphasis added).

Clearly, Hashimoto discloses connecting the switches to a single pin of an IC, which is the conventional approach. Switches S1 and S2 referred to by Hashimoto are part of testing apparatus 20 and, contrary to the present invention, are not part of IC under test 10. This is clear from all of the figures of Hashimoto. Thus, the Hashimoto invention necessarily suffers from the same disadvantages as the admitted art discussed above and does not overcome the problem Applicant seeks to overcome.

The Hashimoto invention is generally described in the first full paragraph of the Summary of the Invention in column 4 of the patent. The paragraph reads as follows:

> "The present invention relates to an IC testing apparatus including a DC tester having voltage measuring means and a current source for executing a DC test of an IC under test by connecting the voltage measuring means and the current source to a terminal of an IC under test through a first switch and a second switch respectively. In accordance with the invention, the first and the second switch both comprise semiconductor switches, and a third switch ~~the second switch~~ is connected [sic] across their terminals located toward the direct current tester. A functional tester which executes a functional test of an IC under test is connected to the terminal of the IC under test through a fourth switch, which may comprise a semiconductor switch as required." (Note the error in the paragraph.)

This is not the invention proposed by Applicant. The present invention does not provide a switch across "the terminals of the first and second switches located toward the direct current tester" of the IC testing apparatus, as required by Hashimoto. More importantly, Hashimoto is not concerned with applying a stimulus voltage to a node within a circuit. As in the admitted art, both switches are connected to a single terminal of the IC, not to separate pins of the IC, as set forth in amended claim 1.

Claims 2-6 depend directly or indirectly from claim 1 and, therefore, patentably distinguish from the applied art for the same as well as for other reasons. The features set forth in these claims are not disclosed in the references and can only be considered obvious in hindsight with the benefit of Applicant's specification, which is improper.

With regard to claim 4, the Examiner states that "Hashimoto discloses in Fig. 7 the switching means (S1, S2) being selectively controlled by a periodic signal (produced by controller 50)". Applicant is unable to find any teaching or suggestion in Hashimoto of using a "periodic signal" in the description of Fig. 7 of Hashimoto. In Applicant's view, the four switches are either ON or OFF depending on the type of test to be performed, such as an overload test or a functional test. The Examiner's attention is directed to Col. 8, lines 3-57 reproduced below for the Examiner's convenience:

> "Semiconductor switches used for the first switch S1 to the fourth switch S4 are preferably of a type as mentioned above in connection with FIG. 5 which are turned on and off in response to a light emission from a light emitting element, for example. The first switch S1 and the second switch S2 employ semiconductor switches having a reduced off capacitance if their on resistances R1 and R2 are relatively high. For example, the on resistance may be on the order of 20Ω. and the off capacitance is equal to or less than 1 pF. The fourth switch S4 employs a semiconductor switch having an on resistance R4 which is less than the on resistance of each of the first switch S1 and the second switch S2 even though the off capacitance may be greater. There is no particular limitation applied to the third switch S3, but preferably employs a semiconductor switch having a reduced change in the on resistance R3 in order to maintain a constant transmission line impedance.
>
> When conducting a DC test in a normal current region on the order of 4 to 50 mA, a controller 50 controls the switches so that the first switch S2 and the second switch S2 are turned on while the third switch S3 and the fourth switch S4 are turned off. Accordingly, a current IS is supplied from a current source 31 to an IC under test 10 through a force line FOR, and a voltage developed at the terminal P while the current IS is being passed can be accurately measured by voltage measuring mean 32 through a sense line SEN. Thus, this test remains the same as the current-applied voltage measuring test mentioned previously in connection with FIG. 1.
>
> On the other hand, when conducting a current-applied voltage measuring test under an overload condition, the controller 50 controls the fourth switch S4 to be turned on also. Under this condition, the first switch S1 and the sense line SEN associated with the voltage measuring means are connected to the current source 31 through the fourth switch S4, and the first switch S1 and the second switch S2 are connected in parallel relationship to each other through the fourth switch S4. Accordingly, if the first switch S1 and the second switch S2 had substantially equal on resistances, the parallel connection results in reducing the equivalent on resistance presented by the first switch S1 and the second switch S2 to be reduced to nearly one-half, allowing an increased current flow from the

current source 31 to the terminal P. To accomplish such an effect, it is preferred that the on resistance of the fourth switch S4 be by an order of magnitude or more less than the on resistance of the first switch S1 and the on resistance of the second switch S2. During the functional test, both the first switch S1 and the second switch S2 are turned off, and because the off capacitances of the first switch S1 and the second switch S2 are reduced as may be exemplified by their values equal to or less than 1 pF, they present a sufficiently high impedance to prevent a test pattern signal from passing into the DC tester 30, thus avoiding the likelihood of causing a degradation in the waveform of the test pattern signal." (emphasis added).

Clearly, it is contrary to the teachings of Hashimoto to control the switches using a periodic signal – the state of the switches depends on the test being performed.

In summary, Applicant respectfully submits that claim 1 and its dependent claims 2-6 and new claim 13 are patentable over the admitted art and Hashimoto.

Allowable Subject Matter

Applicant notes with appreciation the indicated allowability of claims 7-9.

Early favorable reconsideration and allowance of the application is respectfully requested.

Respectfully Submitted,

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